UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/640,961	08/16/2000	Qing Ma	p9556	3719

92265 7590 07/25/2012

Winkle, PLLC
c/o CPA Global
P.O. Box 52050
Minneapolis, MN 55402

EXAMINER	
CLARK, SHEILA V	
ART UNIT	**PAPER NUMBER**
2896	

MAIL DATE	DELIVERY MODE
07/25/2012	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte QING MA, XIAO-CHUN MU, and HARRY H. FUJIMOTO

Appeal 2011-011847
Application 09/640,961
Technology Center 2800

Before JOHN A. JEFFERY, THOMAS S. HAHN, and JENNIFER S. BISK, *Administrative Patent Judges*.

BISK, *Administrative Patent Judge*.

DECISION ON APPEAL

DECISION ON APPEAL

This is an appeal under 35 U.S.C. § 134(a) from the Examiner's final rejection of all pending claims 1-4, 24-29, 31, and 33-40. Br. 5. Claims 5-23 have been withdrawn. *Id.* Claims 30 and 32 have been canceled. Amendment filed 11/9/2009. We have jurisdiction under 35 U.S.C. § 6(b).

We affirm.

STATEMENT OF THE CASE

Appellants' invention relates to "apparatus and processes for packaging microelectronic dice. In particular, the present invention relates to a packaging technology that fabricates build-up layers on encapsulated microelectronic dice and on the encapsulation material which covers the microelectronic dice." Spec. 1. Claim 1, reproduced below with emphases added, is illustrative of the claimed subject matter:

> 1. A microelectronic package, comprising:
>
> a microelectronic *die having an active surface* and at least one side;
>
> encapsulation material adjacent said at least one microelectronic die side, wherein said encapsulation material includes at least one surface substantially planar to said microelectronic die active surface;
>
> a first dielectric material layer disposed on at least a portion of said microelectronic die active surface and said encapsulation material surface; and
>
> *at least one first conductive trace* disposed on said first dielectric material layer and *in physical and electrical contact with said microelectronic die active surface*, wherein said at least one first conductive trace extends adjacent said microelectronic die active surface and adjacent said encapsulation material surface.

THE REJECTIONS

1. Claims 1 and 31 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Fordemwalt (US 3,407,479; Oct. 29, 1968). Ans. 8-10.
2. Claims 26 and 27 stand rejected under 35 U.S.C. § 103(a) as being obvious over Fordemwalt. Ans. 9-10.
3. Claims 1, 4, 24, 26, 27, 31, 35, 36, and 38 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Donovan (US 3,343,255; Sept. 26, 1967). Ans. 12-14.
4. Claims 1-4, 25, 26-29, 31, 33-35, and 37-40 stand rejected under 35 U.S.C. § 103(a) as being obvious over Chung (US 6,288,905 B1; Sept. 11, 2001). Ans. 4-8, 15-16.
5. Claim 1 stands rejected under § 102(a) as being anticipated by Nishihara (US 6,013,953; Jan. 11, 2000). Ans. 11.
6. Claims 26 and 27 stand rejected under § 103(a) as obvious over Nishihara. Ans. 11-12.
7. Claims 4, 24, 35, and 36 stand rejected under 35 U.S.C. § 103(a) as being obvious over Chung or Nishihara or Fordemwalt and Donovan. Ans. 16-17.

ANALYSIS

Rather than repeat the arguments of Appellants or of the Examiner, we refer to the Brief and the Answer for their respective details. In this decision, we have considered only those arguments actually made by Appellants. Arguments that Appellants could have made but did not make in the Brief have not been considered and are deemed to be waived. *See* 37 C.F.R. § 41.37(c)(1)(vii) (2010).

Appellants do not address rejection 5 at any point in their Appeal Brief. *See generally* Br. We therefore summarily affirm the Examiner's rejection of claim 1 as anticipated by Nishihara. *See In re Berger*, 279 F.3d 975, 984-85 (Fed. Cir. 2002) (holding that the Board did not err in sustaining a rejection when the applicant failed to contest the rejection on appeal); MPEP § 1205.02 ("If a ground of rejection stated by the examiner is not addressed in the appellant's brief, that ground of rejection will be summarily sustained by the Board.").

Appellants argue that rejections 1-4, 6, and 7 above should be reversed because each of the four cited references, Fordemwalt, Donovan, Chung, and Nishihara do not disclose at least one of the required limitations. We are not persuaded by Appellants' arguments. For clarity, we address the pivotal issues presented for each of the disputed rejections below grouped by the cited prior art.

THE FORDEMWALT REJECTIONS

Appellants assert that Fordemwalt fails to teach all the limitations of the rejected claims. Specifically, Appellants argue that "Fordemwalt does not show a die side, as he illustrates 'islands' (e.g. column 2, line 47) in a single wafer with 'cut-away' edges that are indeterminate as to where the die side is." Br. 13, 17.

The Examiner, in response, reasonably finds that Fordemwalt "shows microelectronic die in the form of at least one transistor" and shows that "each of said devices formed with . . . at least four sides including a top side where said trace is clearly shown." Ans. 17 (citing Fordemwalt col. 4, l. 42; Fig. 1; elements 13, 14, 15, and 16). Appellants do not dispute this finding.

Thus, based on the record before us, we sustain the Examiner's (1) anticipation rejection of claims 1 and 31 and (2) obviousness rejection of claims 26 and 27, which rely on the same arguments made for claims 1 and 31. Br. 17.

THE DONOVAN REJECTIONS

In rejecting claims 1, 4, 24, 26, 27, 31, 35, 36, and 38 as anticipated by Donovan, the Examiner equates element 32 of Figure 4 to the claimed "at least one first conductive trace." Ans. 12.

Appellants assert that Donovan fails to describe every required limitation of representative claim 1. Br. 14. Specifically, Appellants argue that the Examiner's interpretation of the claim term "trace" is unduly broad. Br. 14. Without providing a specific interpretation of the term, Appellants contend that the "ordinary and customary meaning of the claim term 'trace' is the meaning that the term would have to a person of ordinary skill in the art as defined and demonstrated in Harper." Br. 13-14 (citing Charles A. Harper, ELECTRONIC PACKAGING AND INTERCONNECTION HANDBOOK (3d ed. 2000)). According to Appellants, the Examiner's reference to Donovan's "contact 32" "is not a trace as taught, claimed, and understood by persons of ordinary skill in the art." Br. 14.

The Examiner responds that the Harper reference does not provide a specific definition of the term "trace," but instead simply uses the term in reference to components in specific examples. Ans. 18. We agree with the Examiner that the portions of Harper cited by Appellants do not provide a definition of "trace." *See* Harper at 11.4.4.2 ("All traces that cross a bend radius should cross at 90º to the bend for longest service life."); Figures

14.2, 14.10; 11.2.1.3 (describing a Ball Grid Array Package as including "trace lengths are calculated from the wire bond fingers to the edge placed or custom placed vias."). Nowhere in the portions of Harper on record is there any indication that the trace examples discussed represent the full scope of what a person of ordinary skill in the art would consider a trace. *See* Harper §§ 11.4.4, 14.2.1, 14.2.2, 14.2.3, 14.2.5.

The Examiner also finds that the Specification "fails to provide a specific definition of trace but shows various variations and configurations of trace 208, 234, 276 (shown in the prior art views) and 124, 132 each shown as a wiring segment or wiring pattern on a substrate." Ans. 18. Thus, the Examiner adopts a reasonably broad interpretation of the claim term "trace," finding that "[t]race is [a] term known in this art as a conductive or metallization pattern formed on a substrate and may have various configurations. . . . [a] trace may be an electrode or bond pad or other type of conductive interconnect pattern." Ans. 17 (citing www.4pcb.com, www.trianglecircuits.com). Other than the reference to Harper, which we do not find persuasive, Appellants provide no persuasive evidence or rationale to show this interpretation is incorrect. Thus, based on the record before us, we agree with the Examiner's interpretation. Appellants do not dispute that the Examiner's definition of trace includes contact 32 of Donovan.

Appellants argue that claim 24 is patentable for the additional reason that it fails to teach "said encapsulation material is adjacent at least a portion of said at least one heat dissipation device." Br. 14. Appellants support this assertion by stating, without citation to the record, that "[t]he Examiner previously admitted this deficiency in Donovan." *Id.* Appellants provide no indication of why they believe Donovan does not teach this limitation. The

Examiner does not agree in the Answer that Donovan fails to teach this limitation. Instead, the Examiner finds that "Donovan . . . teaches a heat dissipation device 40 in thermal contact with the back surface of the microelectronic device." Ans. 18. Appellants do not address this finding.

For the foregoing reasons, we sustain the Examiner's anticipation rejections of (1) representative claim 1 and (2) dependent claim 24, and (3) claims 2-4, 26, 27, 31, 35, 36, and 38, which were not argued separately with particularity. Br. 14.

THE CHUNG REJECTIONS

In rejecting claims 1-4, 25-29, 31, 33-35, and 37 as obvious over Chung, the Examiner equates element 144 of Chung to the claimed "at least one first conductive trace." Ans. 4.

Appellants argue that "Chung's 'bump 144' cannot be construed as a trace as it is understood by persons of ordinary skill in the art" because "the 'first conductive trace' is a single structure with no junctions." Br. 15-16 (citing Harper § 14.2.2.1, 14.2.1.3, 14.2.2.4, Figure 14.10). In addition, Appellants argue that "bump 144" is not in "physical contact" with the active surface as required. *Id.* Instead, Appellants assert that "bump 144" is in physical contact with "'contact pad 142b.'" Br. 16. Further, Appellants assert that "Chung's trace 110 is not 'in physical and electrical contact' [with] Chung's active surface" because "[s]everal intervening structures are between Chung's trace 110 and Chung's active surface." Br. 15.

For the reasons discussed above with respect to the Harper reference, we agree with the Examiner that the broadest reasonable interpretation of "trace" includes element 144. We also find reasonable the Examiner's

findings that "Chung et al teaches that said bump 144 is formed integrated with an interconnect (trace) as shown by 26 in prior art figure 1 and figure 5" and "figure 14 shows . . . at least one trace 114a or 114b (having an integrated bump) disposed on the dielectric material and clearly shown in contact with the active surface of die 140." Ans. 19. Appellants do not rebut these findings.

Therefore, based on the record before us, we sustain the Examiner's obviousness rejections of claim 1 and claims 2-4, 25-29, 31, 33-35, and 37, which were not argued separately with particularity. Br. 15-17.

THE NISHIHARA REJECTIONS

In rejecting claims 26 and 27 as obvious over Nishihara, the Examiner equates element 2 of Nishihara to the claimed "at least one first conductive trace." Ans. 11.

Appellants argue that trace 2 of Nishihara is not in physical and electrical contact with said microelectronic die active surface as required by the claims. Br. 17. Instead, Appellants assert that only "bond pad 9" of Nishihara is in physical contact with the die active surface. *Id.* For the same reason, Appellants assert that trace 2 is not "disposed on the first dielectric material (adhesive 3) which is on the active surface of the chip 1." Br. 17.

For the reasons discussed above with respect to the Harper reference, we agree with the Examiner that the broadest reasonable interpretation of "trace" includes trace 2. We also find reasonable the Examiner's finding that the "bond pad and trace of Nishihara are deemed to be integral structures necessary to provide contact to the active surface." Ans. 20. Appellants do not rebut this finding.

Therefore, based on the record before us, we sustain the Examiner's obviousness rejections of claim 26 and 27.

THE REMAINING REJECTION

Appellants argue that the Examiner's rejection of claims 4, 24, 35, and 36 as obvious over a combination of Chung, Nishihara, or Fordemwalt combined with Donovan should be reversed because "[n]one of the references alone or in combination teach a trace as claimed and as understood by persons of ordinary skill in the art" because "what teaching Donovan et al. adds to teach a heat dissipation device, does not amount to a teaching or suggestion of all the limitations of claims 4, 24, 35, and 36." Br. 18. Appellants add that heat dissipation is not mentioned in Chung or Donovan and the Examiner "has used the Appellants' disclosure as a guide to make the claimed combination." *Id.*

In response, the Examiner explains that "Donavan [sic] has been used to show the well known [sic] use of heat dissipation devices attached to semiconductor devices (i.e. [sic] microelectronic dies)" and "[i]t is further well known [sic] to form a plurality of dielectric layers on the surfaces of chips having metallization or traces formed thereon." Ans. 20. Appellants do not rebut this finding. We agree with the Examiner. *See*, *e.g.*, Donovan, col. 4, ll. 21-24 ("On the bottom surface of the device is shown a thermally conductive member **40** bonded to the structure by a suitable metallic solder **42** that will facilitate heat dissipation.").

For the foregoing reasons, we sustain the Examiner's obviousness rejection of claims 4, 24, 35, and 36.

DECISION

The Examiner's decision rejection claims 1-4, 24-29, 31, and 33-40 is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

gvw